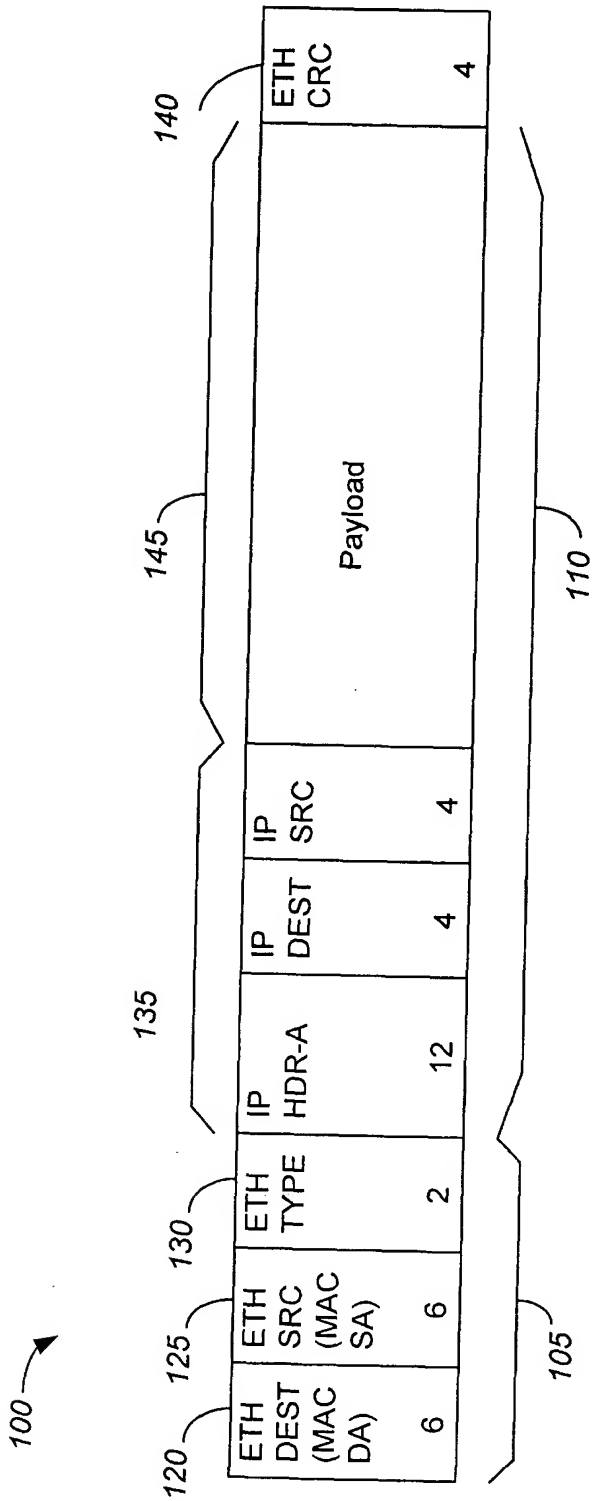


FIG. 1
(PRIOR ART)

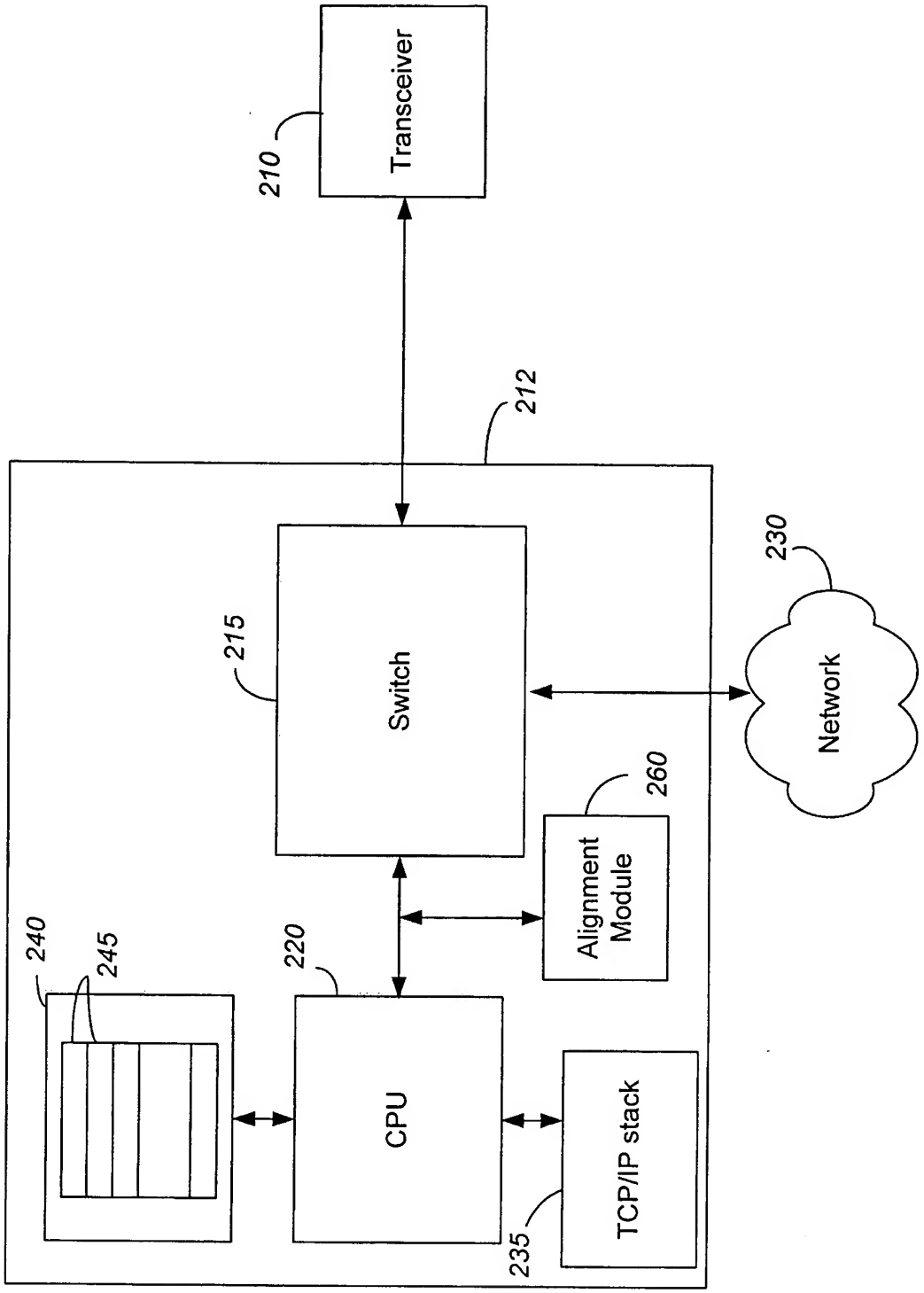
Transceiver
210
212
Switch
215
230
Network
260
Alignment Module
240
245
220
CPU
TCP/IP stack
235

FIG. 2

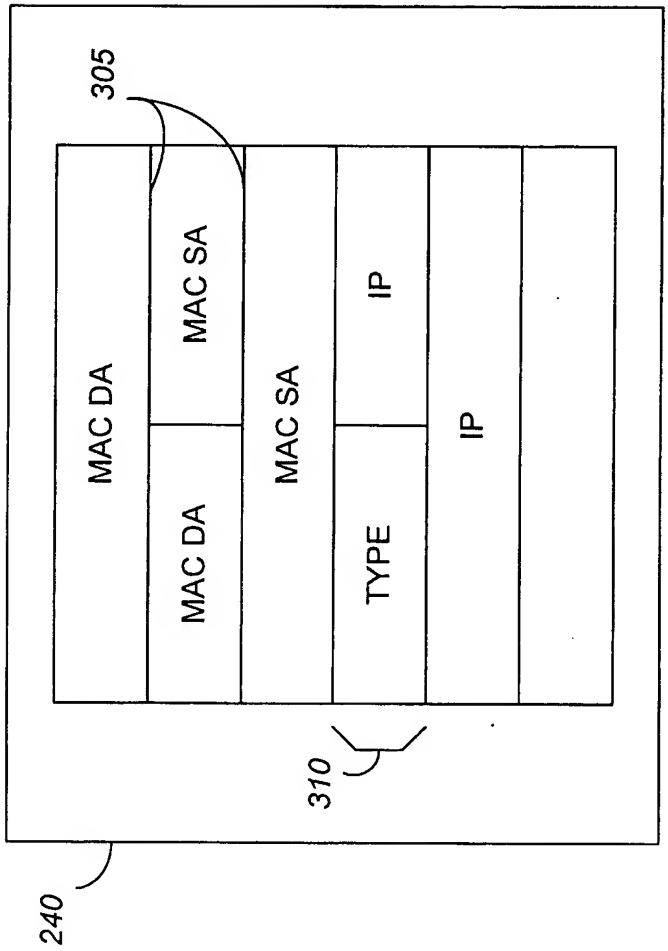


FIG. 3

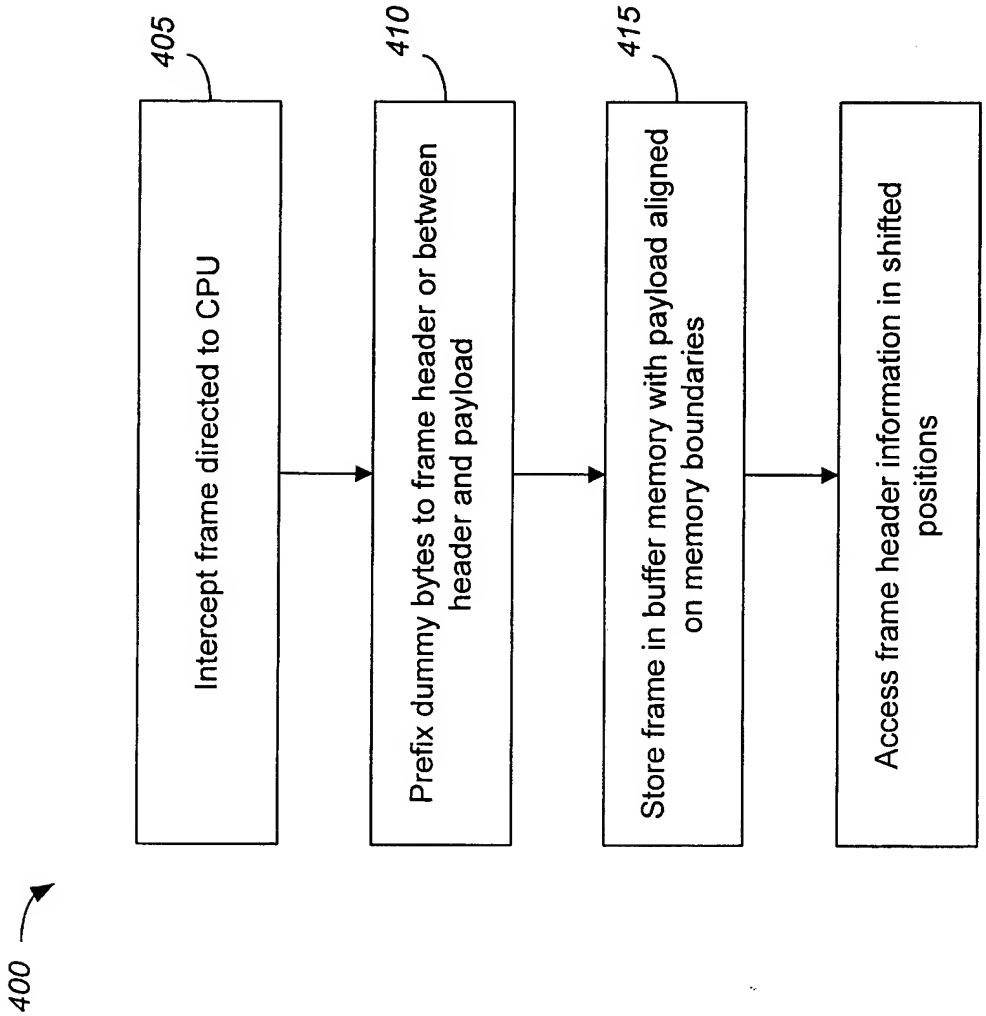
400
405
Intercept frame directed to CPU
410
Prefix dummy bytes to frame header or between header and payload
415
Store frame in buffer memory with payload aligned on memory boundaries
Access frame header information in shifted positions

FIG. 4

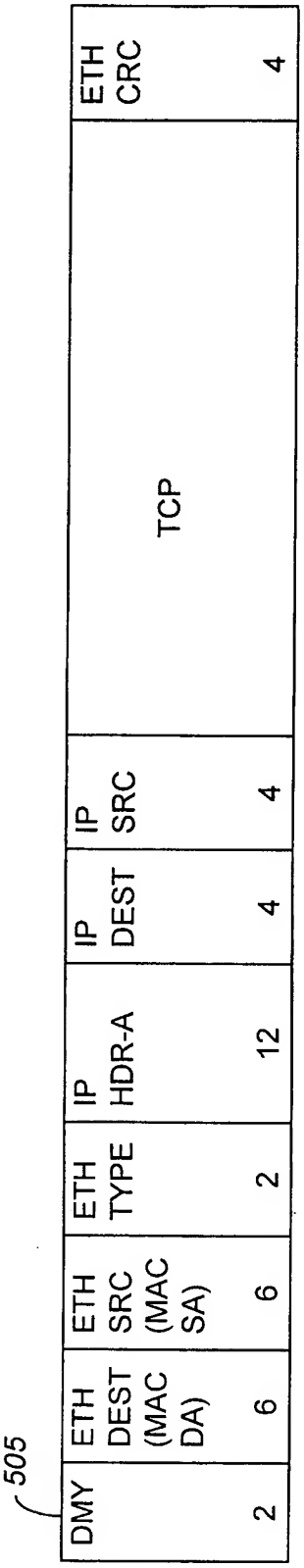
505
DMY
2
ETH DEST (MAC DA)
6
ETH SRC (MAC SA)
6
ETH TYPE
2
IP HDR-A
12
IP DEST
4
IP SRC
4
TCP
ETH CRC
4

FIG. 5

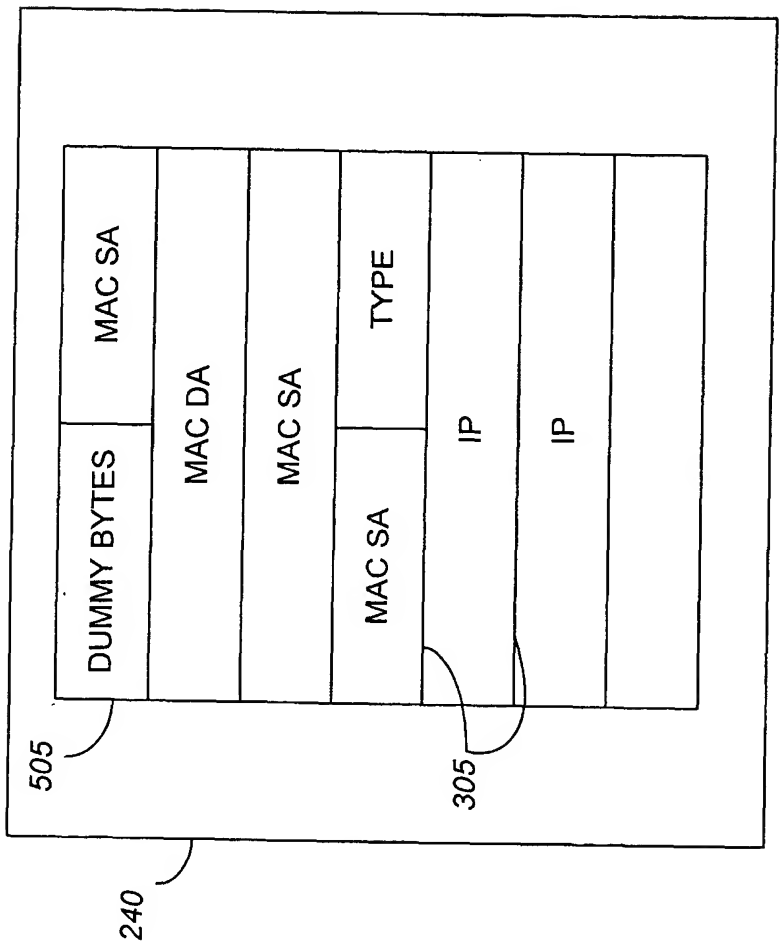


FIG. 6

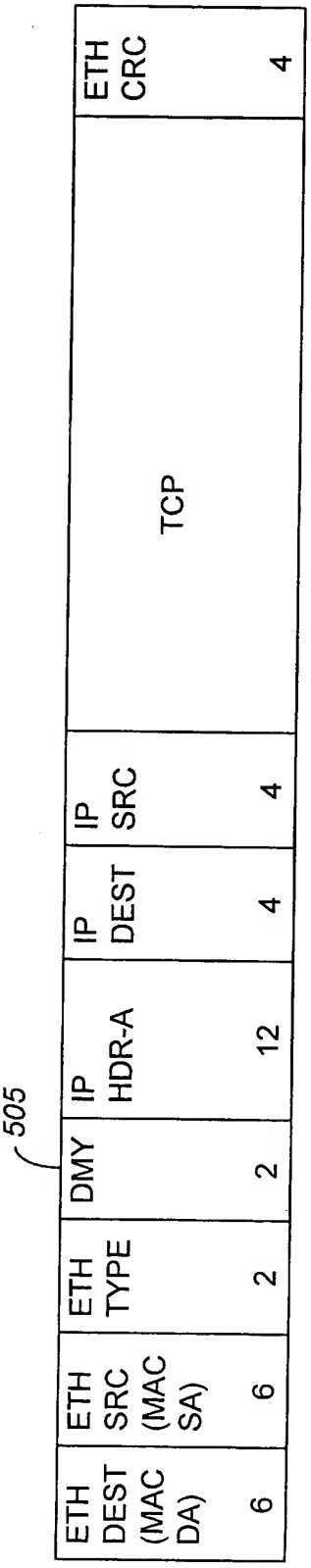
505
ETH DEST (MAC DA)
6
ETH SRC (MAC SA)
6
ETH TYPE
2
DMY
2
IP HDR-A
12
IP DEST
4
IP SRC
4
TCP
ETH CRC
4

FIG. 7